RCBus Specification Notes

The following notes describe limitations in the current RCBus specification and ideas being considered for future updates of the specification.

It is recommended that anyone wishing to add functions to the RCBus, either just for their own use or as prototypes for future additions to the specification, consider following any suggestions in this document, unless there is a good reason not to.

It is also recommended that any thoughts about adding functions to the RCBus be shared on the retro-comp google group in order to bring together the best ideas, improve the specification, and avoid compatibility issue.

Z80 family DMA signals

For Tadeusz Pycio:

DMA chips in the Zx80 family:
Z80 DMA - /RDY signal (input, active Low or High).
Z180 - /DREQ0, /DREQ1 (input, active Low), /TEND0, /TEND1 Transfer End 0 and 1 (outputs, active Low)
Z280 - /RDY 0-4 (input, active Low)
There are more bus control signals in the Z280 (/DMASTB, /EOP, global bus control signals /GREQ, /GACK), but these are specific to this processor and I see no need to add them.

I propose to add request signals (input, active Low) for DMA circuits, and two optional DMA output signals.

I see there are no suggestions, so I will try to give my own:
pin 45 - DREQ1; DMA chip input signal, requests generated by I/O device (RDY output signal)
pin 46 - DACK1/TEND1; DMA chip output signal, acknowledgements of service request acceptance or transfer termination (depending on the application in question)
pin 47 - DREQ2
pin 48 - DACK2/TEND2

3v3 supply

This has been considered but the current thinking is to generate this on any module that requires it and not distribute it on the bus. One reason for rejecting the idea was existing backplanes do not have spare tracks suitable for power supplies. During this discussion one suggested pin for a 3v3 supply was pin 41. Another suggestion was to combine two pins for greater capacity, such as pins 40 and 80.